UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,953	12/09/2003	Jason Nathaniel Dale	AUS920030582US1	3694

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/730,953	DALE ET AL.
	Examiner	Art Unit	
	Michael Krofcheck	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>09 December 2003</u>.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-20 and 22-31</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1,5,6,8,10-16,18,22-25,27,30 and 31</u> is/are rejected.

7) ☒ Claim(s) <u>2-4,7,9,11,12,17,19,20,26,28 and 29</u> is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on <u>09 December 2003</u> is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to application 10/730,953 filed on 12/9/2003.

2.   Claims 1-20, 22-31 have been submitted for examination.

3.   Claims 1-20, 22-31 have been examined.

4.   The examiner would like to note that the numbering of the claims omits a claim number 21.

Claim Rejections - 35 USC § 112

5.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6.   Claims 10-12 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7.   Regarding claim 10, it is unclear to the examiner what the applicant is claiming. does the EA get written in the ERAT table by determining if it is translation-disabled or not? If so, where in the specification does it talk of writing an EA by determining if it is translation-disabled or not. Is the applicant claiming that the process of writing an EA include determining if the EA is translation-disabled or not? Did the applicant intend to state the writing of the EA and the determining as two separate processes, like stated in claims 18 and 27?

8.   Claims 11-12 are rejected due to their dependency.

Claim Rejections - 35 USC § 102

9.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10.   Claims 1, 5-6, 8, 15-16 rejected under 35 U.S.C. 102(b) as being anticipated by

Kalyanasundharam, U.S. Patent Application Publication 2002/0133685.

11.   With respect to claim 1, Kalyanasundharam teaches of a method of efficiently

storing an effective address (EA) in an effective to real address translation (ERAT) table

supporting multiple page sizes (fig. 2; item 200), the method comprising the steps of:

adding page size indicator (PSI) fields, based on the number of unique page sizes

supported, to each ERAT entry (figs. 2, 3A; paragraph 0015, 0019; where for N different

page sizes, there are N-1 size-field bits in each entry in the RAM of the TLB);

storing an EA using one ERAT entry (fig. 2; paragraph 0015, 0037; an entry in

the virtual address tag entry in the CAM corresponds to the physical address entry in

the page table array, RAM, and the overall entry (CAM entry and page table entry)

includes the size and the virtual and physical addresses. It is abundantly clear to one of

ordinary skill in the art that only one entry in the CAM and page table array corresponds

to a specific virtual address (EA)); and

setting the PSI fields of the ERAT entry to indicate the page size (figs. 3A-C;

paragraph 0039-0041; where the size bits (PSI fields) in each entry are set in by the

table in fig. 3A to indicate the page size).

12.   With respect to claim 5, Kalyanasundharam teaches of all the limitations of the parent claims as discussed supra. Kalyanasundharam also teaches of wherein a PSI field is added for each unique page size, but not for the base page size (paragraph 0015, 0019; since when N different page sizes are supported, N-1 size-field bits are used, when only the base size is supported, there are no size fields used).

13.   With respect to claim 6, Kalyanasundharam teaches of all the limitations of the parent claims as discussed supra. Kalyanasundharam also teaches of wherein a translation-disabled indicator (TDI) is used to indicate that the ERAT entry for a translation-disabled address does not need translation (figs. 2, 7; item 207; paragraph 0052-53; where the translation bypass bypasses the translation operation, outputting the virtual address from the TLB).

14.   With respect to claim 8, Kalyanasundharam teaches of all the limitations of the parent claims as discussed supra. Kalyanasundharam also teaches of wherein the effective address (EA) is translated to a real address (RA) using the ERAT table (fig. 2; paragraph 0015; where the TLB (ERAT table) translates virtual addresses (EA) into physical addresses (RA)).

15.   With respect to claims 15-16, Kalyanasundharam teaches of all the limitations of each claim as cited with respect to claims 1 and 8, respectively.

Claim Rejections - 35 USC § 103

16.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   .Considering objective evidence present in the application indicating obviousness or nonobviousness.

18.   This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19.   Claim 10, 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam, U.S. Patent Application Publication 2002/0133685 and Kongetira, U.S. Patent 6,078987.

20.   With respect to claim 10, Kalyanasundharam teaches of the limitations of the parent claim as discussed supra. Kalyanasundharam fails to explicitly teach of wherein

the EA is written to the ERAT entry by determining whether the EA is translation-disabled.

However, Kongetira teaches of wherein the EA is written to the ERAT entry by determining whether the EA is translation-disabled (fig. 3, 5-6; column 9, line 64-column 10, line 35; where based on a write enable signal to the CAM, RAM1, and RAM2, the new virtual address and rest of the entry is written. Shown in figs. 5 and 6, the read and write enable signals are not activated at the same time, thus reading out (translation) the data cannot occur when writing it).

Kalyanasundharam and Kongetira are analogous arts as they are both in the same field of endeavor, translation look-aside buffers. It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam and Kongetira at the time of the invention to provide for reading/writing to the CAM and RAM cells of Kalyanasundharam as taught in Kongetira. Their motivation would have been to provide unified array access for the two separate arrays, Kongetira column 6 lines 53-62.

21.   With respect to claim 18, Kalyanasundharam teaches of the limitations of the parent claim as discussed supra. Kalyanasundharam also teaches of the apparatus further comprises means for determining whether the EA is translation-disabled (fig. 2, 7; paragraph 0052-0053). Kalyanasundharam fails to explicitly teach of wherein the EA is written to the ERAT table. However, Kongetira teaches of wherein the EA is written to the ERAT table (fig. 3, 5-6; column 9, line 64-column 10, line 35; where based on a

write enable signal to the CAM, RAM1, and RAM2, the new virtual address and rest of the entry is written).

22.   Claim 13-14, 22-23 rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam, U.S. Patent Application Publication 2002/0133685 and Matthews, U.S. Patent 6,625,715.

23.   With respect to claim 13, Kalyanasundharam teaches of all the limitations of the parent claims as discussed supra. Kalyanasundharam teaches of a conventional valid bit (fig. 2; item 208; paragraph 0038). Kalyanasundharam fails to explicitly teach of wherein the ERAT entry is invalidated.

However, Matthews teaches of wherein the ERAT entry is invalidated (fig. 7, column 9, line 54-column 10, line 8).

Kalyanasundharam and Matthews are analogous arts as they are both in the same field of endeavor, address translation with multiple size pages. It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam and Matthews at the time of the invention to incorporate the CAM purging array and method of using it from Matthews into Kalyanasundharam to purge an entry by toggling the valid bit of the entry. Their motivation would have been to remove old/unused entries to make room for new entries.

24.   With respect to claim 14, the combination of Kalyanasundharam and Matthews teaches of all the limitations of the parent claims as discussed supra. Kalyanasundharam also teaches of means for dividing the EA into ranges based upon how many page sizes are supported (figs. 2, 8-9b; paragraph 0055-0058; where the

CAM is used to enable optional matching of certain bits, particularly, VA[21:19], VA[18:16], and VA[15:13]);

means for comparing the EA to each entry in the ERAT (figs. 2, 8-9b; paragraph 0055-0058; where the CAM is used to enable optional matching of certain bits, particularly, VA[21:19], VA[18:16], and VA[15:13]);

means for determining which EA ranges should match in order for the EA to match the ERAT entry by checking the PSI fields for each ERAT entry (figs. 2, 8-9b; paragraph 0055-0058; where the X and Y-bit latches are used to encode if a particular bit should be ignored during the match. As this is determined based on the page size, and the page size is shown by the size bits, the status of the X and Y-bits are determined by the size bits (PSI fields));

Kalyanasundharam fails to explicitly teach of upon determining the EA matches an ERAT entry, means for setting an invalid indicator field in the ERAT entry. However, Matthews teaches of upon determining the EA matches an ERAT entry, means for setting an invalid indicator field in the ERAT entry (fig. 7; items 780, 756; column 9, line 54-column 10, line 8).

25.   With respect to claims 22 and 23, Kalyanasundharam teaches of all the limitations of the parent claims, as discussed supra.   The combination of Kalyanasundharam and Matthews teaches of all the limitations cited in each claim, cited with respect to claims 13 and 14 respectively.

26.   Claim 24-25 rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam, U.S. Patent Application Publication 2002/0133685 and Lomax, JR. et al., U.S. Patent Application Publication 2003/0204702 (hereinafter Lomax).

27.   With respect to claims 24-25, Kalyanasundharam teaches of the limitations cited above with respect to claims 1 and 8, respectively. Lomax teaches of implementing a machine-readable medium containing instructions (paragraph 0017).

Kalyanasundharam and Lomax are analogous arts as they are both in the same field of endeavor, translation look-aside buffers. It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam and Lomax at the time of the invention to implement the invention of Kalyanasundharam as instructions on a computer readable medium. Their motivation would have been to allow for upgrades and changes to be implemented without changing the hardware.

28.   Claim 27 rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Lomax as applied to claim 24 above, and further in view of Kongetira.

29.   With respect to claim 27, the combination of Kalyanasundharam and Lomax teach of the limitations of the parent claims as discussed supra. Kalyanasundharam also teaches of determining whether the EA is translation-disabled (fig. 2, 7; paragraph 0052-0053). Lomax teaches of implementing a machine-readable medium containing instructions (paragraph 0017). The combination of Kalyanasundharam and Lomax fails to explicitly teach of wherein the EA is written to the ERAT table. However, Kongetira teaches of wherein the EA is written to the ERAT table (fig. 3, 5-6; column 9, line 64-

column 10, line 35; where based on a write enable signal to the CAM, RAM1, and RAM2, the new virtual address and rest of the entry is written).

The combination of Kalyanasundharam and Lomax, and Kongetira are analogous arts as they are both in the same field of endeavor, translation look-aside buffers. It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam, Lomax and Kongetira at the time of the invention to provide for reading/writing to the CAM and RAM cells of the combination Kalyanasundharam and Lomax as taught in Kongetira. Their motivation would have been to provide unified array access for the two separate arrays, Kongetira column 6 lines 53-62.

30.   Claim 30-31 rejected under 35 U.S.C. 103(a) as being unpatentable over Kalyanasundharam and Lomax as applied to claim 24 above, and further in view of Matthews.

31.   With respect to claims 30-31, the combination of Kalyanasundharam and Lomax teach of the limitations of the parent claims. The combination of Kalyanasundharam and Lomax also teach of limitations cited with respect to claims 13-14 respectively. Matthews teaches of limitations cited with respect to claims 13-14, respectively.

The combination of Kalyanasundharam and Lomax, and Matthews are analogous arts as they are both in the same field of endeavor, address translation with multiple size pages. It would have been obvious to one of ordinary skill in the art having the teachings of Kalyanasundharam, Lomax, and Matthews at the time of the invention to incorporate the CAM purging array and method of using it from Matthews into the

combination of Kalyanasundharam and Lomax to purge an entry by toggling the valid bit

of the entry. Their motivation would have been to remove old/unused entries to make

room for new entries.

Allowable Subject Matter

32.   Claims 2-4, 7, 9, 17, 19-20, 26, 28-29 objected to as being dependent upon a

rejected base claim, but would be allowable if rewritten in independent form including all

of the limitations of the base claim and any intervening claims.

33.   Claims 11, 12 would be allowable if rewritten to overcome the rejection(s) under

35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the

limitations of the base claim and any intervening claims.

34.   The following is a statement of reasons for the indication of allowable subject

matter:

   a.   With respect to claims 2-4, the prior art of Kalyanasundharam teaches of

the limitation of claim 5, and teaches of using 2 fields to indicate 4 unique page

sizes (fig. 1A), but fails to teach of wherein a PSI field is added for each unique

page size, including the base page size.

   b.   With respect to claim 7, the prior art of Kalyanasundharam teaches of

when translation is disabled, outputting the virtual address; but does not teach of

a translation-disabled address not being stored in the ERAT.

   c.   With respect to claims 9, 17, 26, the prior art, previously mentioned,

teaches of dividing the EA into ranges, based on the number of page sizes

supported; comparing the EA to each entry in the ERAT; determining whether the EA is translation-disabled; upon determining the EA is translation-disabled, outputting the EA as the RA, as stated in each claim. The prior art does not teach of upon determining the EA is not translation-disabled, determining which EA ranges should match, in order for the EA to match the ERAT entry, by checking the PSI fields for each ERAT entry as stated in each claim.

d.   With respect to claims 11, 19, 28, the prior art of Kalyanasundharam teaches of determining the page size of the EA, but does not teach of determining the page size of the EA after determining that the EA is not translation-disabled. Kalyanasundharam teaches of processing the translation through the CAM and page table and then selecting the final output based on the translation bypass (fig. 2).

e.   With respect to claims 12, 20, 29, the prior art of Kalyanasundharam teaches of determining whether the EA matches an existing entry, and upon determining such, that entry is used and a new entry is not written, but Kalyanasundharam does not teach of doing it after determining that the EA is translation-disabled.

Conclusion

35.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

36.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

37.   If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

38.   Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michael Krofcheck

MATTHEW D. ANDERSON
PRIMARY EXAMINER